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MANUFACTURE OF MULTILAYERED WIRING BOARD

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ABSTRACT

PROBLEM TO BE SOLVED: To provide a manufacture of a multilayered wiring board capable of raising the density of wiring, without the use of a special insulation material and without the need for large equipment investment.

SOLUTION: In this manufacture, on the surface of an inner layer substrate 4 where an inner layer circuit 3 is formed, an insulating adhesive layer 2 and a conductor metallic foil 1 are laminated in the order, pressed, heated, and intergrated and an opening part 5 is formed at a part for forming an IVH (interstitial via hole) 9 for electrically connecting the conductor metallic foil 1 and the inner layer circuit 3. The method also includes a process for opening a non-through hole 11 by having the opening part 5 irradiated with a laser beam 6, applying a catalyst 7 for plating, forming a plating resist 8 on the surface of the conductor metallic foil 1 excluding the non-through hole 11 and the periphery, performing plating 13 at the part where the plating resist 8 is not formed, removing the plating resist 8, etching and removing the unwanted parts of the conductor metallic ***foil*** 1 and forming an outer layer wiring 10.

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TITLE: Interstitial through hole formation method for multi-layer wiring board manufacturing - involves forming vent on surface at metallic foil and laser is irradiated on vent to form non-through hole

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ABSTRACTED-PUB-NO: JP 11087921A
BASIC-ABSTRACT:

NOVELTY - A vent (5) is formed by etching portion of the foil where an interstitial through hole (9) electrically connected with the inner layer is to be formed. Laser light (6) is radiated to the vent for forming a non-through hole (11) in the cementing layer until inner side layer is exposed. DETAILED DESCRIPTION - An insulating cementing layer (2) and a conductor metallic foil (1) are laminated on the surface of a substrate (4) on which an inner layer (3) is formed. Pressure application and heating process is performed to unify the above structure. A plating catalyst (7) is filled in the inner wall of the non-through hole. A plating resist (8) is formed on the surface of the foil except the non-through hole and its perimeter. A plating (13) is formed in the non-through hole and its perimeter where the resist is not formed. An outer layer wiring (10) is formed on the surface of an insulating cementing layer (2) after removing a plating resist (8) and unnecessary location of a conductor metallic foil (1).

USE - For multilayer wiring board manufacture.

ADVANTAGE - Performs high-density minute wiring with low capital investment as common adhesive agent is used. DESCRIPTION OF DRAWING(S) - The figures show sectional view in each of manufacturing processes of wiring board. (1) Conductor metallic foil; (2) Insulating cementing layer; (3) Inner layer; (4) Substrate; (7) Plating catalyst; (8) Plating resist; (9) Interstitial through hole; (10) Outer layer wiring; (13) Plating.

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CLAIMS

[Claim(s)]

[Claim 1] The manufacturing process of the multilevel interconnection board characterized by including the following processes in the manufacture method of a multilevel interconnection board with IVH (9) for connecting between adjoining layers.

a. Put an insulating adhesive line (2) and conductor metallic foil (1) on the surface of the inner layer board (4) in which the inner layer circuit (3) was formed at this order. The part which forms IVH (9) which carries out pressurization heating and makes electric connection of the process and b. conductor metallic foil (1) to unify, and a inner layer circuit (3), Laser light (6) is irradiated at the process which carries out etching removal of the conductor metallic foil (1), and forms an opening (5), and the opening (5) formed in c. conductor metallic foil (1). The process which makes a non-penetrating hole (11) until a inner layer circuit (3) is exposed to an insulating adhesive line (2), d. The process which gives the catalyst for plating (7) at least to the insulating adhesive line (2) of a non-penetrating hole (11) inner wall, e. Remove a non-penetrating hole (11) and its circumference on the surface of conductor metallic foil (1). The process which forms a plating resist (8), the process which plates in the part in which f. plating resist (8) is not formed (13), the process which removes g. plating resist (8), the process which carries out etching removal of the unnecessary part of h. conductor metallic foil (1), and forms outer layer wiring (10).

[Claim 2] The manufacturing process of the multilevel interconnection board according to claim 1 characterized by including the following processes.

a. Put an insulating adhesive line (2) and conductor metallic foil (1) on the surface of the inner layer board (4) in which the inner layer circuit (3) was formed at this order. The part which forms IVH (9) which carries out pressurization heating and makes electric connection of the process and b. conductor metallic foil (1) to unify, and a inner layer circuit (3), Laser light (6) is irradiated at the process which carries out etching removal of the conductor metallic foil (1),

and forms an opening (5), and the opening (5) formed in c. conductor metallic foil (1). The process which makes a non-penetrating hole (11) until a inner layer circuit (3) is exposed to an insulating adhesive line (2), d. The process which gives the catalyst for plating (7) at least to the insulating adhesive line (2) of a non-penetrating hole (11) inner wall, e. Remove a non-penetrating hole (11) and its circumference on the surface of conductor metallic foil (1). The process which forms a plating resist (8), the process which plates in the part in which f. plating resist (8) is not formed (13), g. The process which removes a plating resist (8), the process which carries out etching removal of the unnecessary part of h1. conductor metallic foil (1), and forms the 1st outer layer wiring, the process which performs the number-of-times repetition of required, Process a - Process h for the j. process a - a process h1.

[Claim 3] The manufacturing process of the multilevel interconnection board according to claim 1 or 2 characterized by replacing with piling up an insulating adhesive line (2) and conductor metallic foil (1) in Process a, and using the insulation adhesive line with conductor metallic foil (12) which these unified.

[Claim 4] It is the manufacturing process of a multilevel interconnection board given in either among Claim 1 -3 characterized by adding the following processes and preparing a penetration hole (14) simultaneously.

- In the process and the - process d of making a penetration hole (14) in Process b or Process c The process which the plating resist formed in the process and the - process e which also give the catalyst for plating to the inner wall of a penetration hole (14) forms as it removes also in a penetration hole (14) and its circumference, and the process which plates also in the inner wall of a penetration hole (14) in the - process f (13).

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] In order that this invention may connect between adjoining layers InterstitialVia It is related with the manufacture method of a multilevel interconnection board with Hole (henceforth IVH).

[0002]

[Description of the Prior Art] In the multilevel interconnection board, as a method of connecting between layers electrically from the former, after making a penetration hole, the technique of carrying out metal plating was in use. However, by this method, since the wiring prohibition field by a penetration hole is in all the layers, it has been the obstacle of high-density-izing, and the method which uses IVH for connecting between adjoining layers in recent years has been put in practical use. As this manufacture method as indicated to JP,H4-148590,A After forming in the surface of a inner layer circuit board the insulating layer which has photosensitivity,

making a non-penetrating hole in the insulating layer on the surface of a substrate of a portion which performs an interlayer connection by the FOTORISO graph method and carrying out metal plating of the hole and the substrate surface, there is the method (the photograph beer method) of carrying out circuit formation of the conductor on the surface of a substrate by the etching method.

[0003] Moreover, as indicated to JP,H4-3637,B [metallic foil and insulating adhesives] After carrying out lamination adhesion in piles, making a hole in the metal layer on the surface of a substrate of a portion which performs an interlayer connection by the etching method, making a non-penetrating hole in the surface of a inner layer circuit board by laser etc. further and carrying out metal plating of the hole and the substrate surface, there is also the method (the laser puncturing method) of carrying out circuit formation of the conductor on the surface of a substrate by the etching method.

[0004]

[Problem to be solved by the invention] Although an insulating layer will be asked for many characteristics, such as FOTORISO nature, insulation, adhesiveness with plating metal, and coat formation nature to a substrate, by the method indicated to JP,H4-148590,A Few, only the present equipment cannot perform what fills all the present, either, but a certain investment like equipment is needed. For example, since solvent development must be adopted and a chlorinated solvent cannot be used from a viewpoint of environmental protection in the development of a FOTORISO process if a material system with few polar groups is chosen, since it is compatible in insulation and FOTORISO nature, perfect explosion protection type equipment is needed using an inflammable solvent. Moreover, by the method indicated to JP,H4-3637,B, in order to attach metal plating further on metallic foil, the thickness of the metal layer used as a conductor circuit is thick, and in forming a circuit by the etching method, a limit is in the miniaturization of a circuit.

[0005] This invention aims at offering the manufacture method of the multilevel interconnection board in which high-density-izing of wiring is possible not using a special insulating material, without needing great plant-and-equipment investment.

[0006]

[Means for solving problem] The manufacturing process of the multilevel interconnection board of this invention is characterized by including the following processes in the manufacture method of a multilevel interconnection board with IVH9 for connecting between adjoining layers.

a. as are shown in drawing 1 (a) and the insulating adhesive line 2 and the conductor metallic foil 1 are shown in the surface of the inner layer board 4 in which the inner layer circuit 3 was formed at the process and b. drawing 1 (b) which pile up and carry out pressurization heating and which are unified in this order As shown in the process and c. drawing 1 (c) which carry

out etching removal of the conductor metallic foil 1 and the conductor metallic foil 1 of the part which forms IVH9 which makes electric connection of the inner layer circuit 3, and form an opening 5 As shown in the process and d. drawing 1 (d) which make the non-penetrating hole 11 until it irradiates the laser light 6 at the opening 5 formed in the conductor metallic foil 1 and the inner layer circuit 3 is exposed to the insulating adhesive line 2 As shown in the process and e. drawing 1 (e) which give the catalyst 7 for plating to the insulating adhesive line 2 of the wall in the non-penetrating hole 11 at least As shown in the process and f. drawing 1 (f) which form the plating resist 8 in the surface of the conductor metallic foil 1 except for the non-penetrating hole 11 and its circumference The process which carries out etching removal of the unnecessary part of the conductor metallic foil 1, and forms the outer layer wiring 10 as shown in the process which carries out plating 13 to the part in which the plating resist 8 is not formed, the process which removes the plating resist 8 as shown in g. drawing 1 (g), and h. drawing 1 (h).

[0007] In order to multilayer, it is possible by performing it as follows.

a. Put the insulating adhesive line 2 and the conductor metallic foil 1 on the surface of the inner layer board 4 in which the inner layer circuit 3 was formed at this order. The part which forms IVH9 which carries out pressurization heating and makes electric connection of the process and b. conductor metallic foil 1 to unify, and the inner layer circuit 3, The laser light 6 is irradiated at the process which carries out etching removal of the conductor metallic foil 1, and forms an opening 5, and the opening 5 formed in c. conductor metallic foil 1. The process which makes the non-penetrating hole 11 until the inner layer circuit 3 is exposed to the insulating adhesive line 2, d. The process which gives the catalyst 7 for plating at least to the insulating adhesive line 2 of the wall in the non-penetrating hole 11, e. The process which forms the plating resist 8 in the surface of the conductor metallic foil 1 except for the non-penetrating hole 11 and its circumference, f. Carry out etching removal of the unnecessary part of the process which carries out plating 13 to the part in which the plating resist 8 is not formed, the process which removes g. plating resist 8, and the h1. conductor metallic foil 1. The process which forms the 1st outer layer wiring, the process which performs the number-of-times repetition of required, Process a - Process h for the j. process a - a process h1.

[0008] Moreover, in Process a, it can replace with piling up the insulating adhesive line 2 and the conductor metallic foil 1, and the insulation adhesive line 12 with conductor metallic foil which these unified can also be used.

[0009] Furthermore, the following processes can be added, and as shown in drawing 2 , the penetration hole 14 can also be formed simultaneously.

- In the process and the - process d of making the penetration hole 14 in Process b or Process c The process which the plating resist 8 formed in the process and the - process e which also give the catalyst for plating to the inner wall of the penetration hole 14 forms as it removes also

in the penetration hole 14 and its circumference, and the process which carries out plating 13 also to the inner wall of the penetration hole 14 in the - process f.

[0010]

[Mode for carrying out the invention]

((a) Process) If wiring formation can be carried out by the etching method, the conductor metallic foil 1 used by this invention is usable, and, generally its copper foil is desirable. Moreover, in order to form detailed wiring, the thinnest possible thing of the thickness of metallic foil is desirable, but when copper foil is a monolayer, and it thinks from handling nature, 9 to 18 micrometers is good. Moreover, when a line/space forms the very detailed wiring below 50 micrometers / 50 micrometers, the still thinner thing of the thickness of copper foil is desirable, and, in such a case, the compound foil which consists of a reinforcing layer of 3-9-micrometer ultra-thin copper foil and its ultra-thin copper foil is used. this reinforcing layer -- after pressurization heating lamination -- tearing off -- it exfoliates or etching removes. There is peeler bull copper foil (the Koga circuit foil incorporated company make, brand name) which tears off and consists of copper foil of 70-micrometer thickness and 9-micrometer ultra-thin copper foil as an example of possible compound foil. As what can remove a reinforcing layer by etching, the compound foil (made by Mitsui Mining & Smelting Industries) from which the aluminum foil which decoded 5-micrometer ultra-thin copper foil is removed by etching is in aluminum foil.

[0011] As resin of the insulating adhesive line 2 used by this invention, resin, such as phenol resin, an epoxy resin, and polyimide resin, can be used. Since this insulating adhesive line 2 carries out pressurization heating, irradiates after lamination and the laser light 6 and makes the hole for an interlayer connection in the inner layer board 4 Since the time which laser processing takes will become long and productivity will become remarkably low if the minerals fiber exceeding the diameter of an interlayer connection is contained in this insulating adhesive line 2, it is desirable not to include the inorganic fiber of the length more than the diameter of the hole made with the laser light 6 in this insulating adhesive line 2. As an insulating adhesive line 2, epoxy and polyimide are included as an ingredient and there is AS-3000E (the HITACHI CHEMICAL CO. LTD. make, brand name) as an epoxy system adhesion film which made the main ingredients the 100,000 or more-molecular weight amount epoxy polymer of polymers. There is GF-3500 (the HITACHI CHEMICAL CO. LTD. make, brand name) as an epoxy system adhesion film which added **** rubber. As a polyimide system adhesion film, there is AS-2500 (the HITACHI CHEMICAL CO. LTD. make, brand name). As an epoxy adhesive film with which the diameter distributed the about 5-100-micrometer-long fibrous substance in epoxy system resin at 0.1-6 micrometers, there is AS-6000E (the HITACHI CHEMICAL CO. LTD. make, brand name). After these insulating adhesive lines 2 apply the varnish which tore off and dissolved thermosetting resin in the solvent on the possible film, they are obtained by

drying a part for a solvent. The thickness of this insulating adhesive line 2 is related to the thickness of the inner layer circuit 3, and it is required from the point of the restoration nature of the inner layer circuit 3 to be more than the thickness of the inner layer circuit 3 at least. When the thickness of the inner layer circuit 3 is 12 micrometers, it is made a thing about 25 micrometers thick. It can be filled up with at least about 10 micrometers of inner layer circuits 3 if it is the thinness whose thickness of the inner layer circuit 3 is about 5 micrometers. Generally the range of the thickness of this insulating adhesive line 2 is 10-500 micrometers.

[0012] [the insulation adhesive line 12 with conductor metallic foil united with the conductor metallic foil 1 which can be replaced with and used for piling up the conductor metallic foil 1 and the insulating adhesive line 2] The thing which was mentioned above on the surface of the conductor metallic foil 1 and which tore off and applied insulating adhesives to the possible film is stuck, and it is obtained by tearing off a film after that. It tears off, an organic film is suitable, and in order to carry out drying by heating removal of the part for a solvent after an application as an organic film which applies adhesives, the heat resistance in this cooking temperature is required for a possible film. As such an organic film, polyethylene terephthalate, polypropylene, 4 MECHIRU pen ten 1 polymer, Pori fluoridation ethylene, etc. can be used. The thickness of these films is 5 micrometers or more, and a certain amount of thickness is required for it from a point of handling nature. Desirable thickness is 10-70 micrometers from such a point.

[0013] Moreover, it is also acquired that this insulation adhesive line 12 with conductor metallic foil applies to direct metallic foil the varnish which dissolved insulating adhesives resin in the solvent. As such a material, there is MCF-3000 (the HITACHI CHEMICAL CO. LTD. make, brand name), for example as an epoxy system adhesion film with copper foil which made the main ingredients the 100,000 or more-molecular weight amount epoxy polymer of polymers. Moreover, there is MCF-6000E (the HITACHI CHEMICAL CO. LTD. make, brand name) as an epoxy adhesive film with copper foil with which the diameter distributed the about 5-100-micrometer-long fibrous substance in epoxy system resin at 0.1-6 micrometers.

[0014] As a inner layer board 4 used by this invention, the one side copper-clad laminate sheet of an epoxy system, a phenol system, and a polyimide system containing a paper base and a glass base material can be used. Moreover, the double-sided copper-clad laminate sheet which consists of these base materials and resin is used. The inner layer circuit 3 is formed using both the etching method or plating and etching using these base materials. Moreover, what formed the conductive pattern with the additive process can be used for the epoxy system, phenol system, and polyimide system board containing a paper base and a glass base material. Moreover, the thing in which the conductive pattern was formed on the surfaces, such as a metal board and a ceramic substrate, can also be used. In the case of the double-sided circuit board by which the inner layer board 4 formed the circuit in the both sides, an interlayer

connection hole uses the double-sided circuit board filled up with a conductive paste or insulating resin.

[0015] Although the conditions which pile up and carry out pressurization heating and which are united with this order depend for the insulating adhesive line 2 and the conductor metallic foil 1 on the resin to be used at this inner layer board 4, generally it is the cooking temperature range of 160-280 degrees C, and, generally pressure is the range of 1-50MPa.

[0016] ((b) Process) Although it is not limited, and especially the hole diameter of the opening 5 prepared in the conductor metallic foil 1 is so good that it is small from a viewpoint of high-density-izing of a substrate, it takes into consideration from the process capacity in the etching method, surroundings nature with plating, etc., and 50 micrometers or more are desirable.

[0017] ((c) Process) Although there are an excimer laser, carbon dioxide laser, etc. as a laser light which irradiates an opening 5, it being easy to process resin layers other than conductor metallic foil 1 alternatively and processing speed are early suitable for the easy carbon dioxide laser of a maintenance. In laser puncturing, the non-penetrating hole 11 can be made until it makes the hole of the same diameter in the insulating adhesive line 2 of the same place as the opening 5 of the conductor metallic foil 1 and the inner layer circuit 3 is exposed by irradiating the laser light of the bigger diameter of a beam than the diameter of an opening 5. Since the laser processing conditions at this time change with the kinds of insulating adhesives layer, they choose an optimal condition experimentally beforehand.

[0018] ((d) Process) [the catalyst 7 for plating given to the insulating adhesive line of the inner wall of the non-penetrating hole 11] As indicated to the method of depositing the detailed metal particles currently generally called ceding and the method of forming a conductive coat, for example, DE 3806884CNo. 1 gazette After making the monomer which consists of a heterocyclic machine of 5 which has nitrogen or sulfur as a different atom, or 6 members adsorb to the resin portion of a hole portion, there is the method of forming a conductive polymer layer etc. by making it polymerize by an oxidizer. In this invention, in order to plate only ****** and the neighborhood of a hole, the method of the latter which can use together electroplating which can be processed at a short process in a short time is desirable. Moreover, in order to raise the adhesion intensity of the catalyst 7 for plating, and a metal plating and the resin layer inside a hole and to raise the reliability for a terminal area, the DESUMIA process which carries out oxidation treatment of the resin layer surface inside a hole before the catalyst grant process for plating can be added.

[0019] ((e) Process) The hole diameter of the plating resist 8 formed in the surface of the conductor metallic foil 1 except for the non-penetrating hole 11 and its circumference is carried out more than the size adding the position ****** error of the hole diameter of the non-penetrating hole 11 formed previously, and the hole established in the plating resist layer formed in the next. It is for the amount of [of a plating layer and the conductor metallic foil 1]

junction to become only the hole end face of the conductor metallic foil 1, and for connection reliability to fall more, in the case of a small hole diameter. As a plating resist 8, what is used for the usual printed circuit board can be used, for example, dry films, such as FOTEKKU H-K425 and FOTEKKU H-W425 (all are the HITACHI CHEMICAL CO. LTD. make and a brand name), can be used.

[0020] ((f) Process) Especially as a method of forming IVH9 which carries out metal plating and connects the inner layer circuit 3 and the conductor metallic foil 1 to the punctured portion, it cannot limit and non-electrolyzed plating or electroplating performed by the usual printed circuit board can be applied.

[0021]

[Working example]

Copper foil thickness as an insulation adhesive line 12 with example 1 conductor metallic foil [12 micrometers] Thickness prepared the epoxy system one side copper-clad laminate sheet circuit processed at 0.2mm as MCF-3000E (the HITACHI CHEMICAL CO. LTD. make, brand name) which is the epoxy system adhesion film with which resin layer thickness made the main ingredients 50 micrometers and the 100,000 or more-molecular weight amount epoxy polymer of polymers, and a inner layer board 4. Next, these were piled up, for 60 minutes, pressurization heating was carried out, pressure 2.5MPa and the temperature of 170 degrees C produced the multilevel interconnection board, and the opening 5 0.1mm in diameter was formed in the surface copper foil coat by the etching method. Next, the non-penetrating hole 11 which irradiates carbon dioxide laser and arrives to the inner layer circuit 3 of the inner layer board 4 was made. Next, the conductive coat was formed in the insulating adhesive line 2 of the non-penetrating hole 11 as a catalyst 7 for plating with DMS-E processing liquid (made in brass Belc OBERUFUREHIENTEHINIKU Gaea M Bex Haar, brand name). Next, as a plating resist 8, after carrying out the heated roll lamination of FOTEKKU H-W425 (the HITACHI CHEMICAL CO. LTD. make, brand name), the mask pattern which forms the non-penetrating hole 11 and a hole with a diameter of 0.3mm containing the circumference was used and developed [exposed and]. Then, 12-micrometer-thick electroplating was performed to non-penetrating hole 11 inside and the circumference, and exfoliation removal of the plating resist 8 was carried out. Furthermore, etching resist was newly formed, the mask pattern was used and developed [exposed and] in the form of the outer layer wiring 10, the circuit of the outermost layer was formed by the etching method, and the two-layer substrate was produced.

[0022] As the peeler bull copper foil (the Koga circuit foil incorporated company make, brand name) which consists of copper foil of the 70-micrometer thickness as a reinforcing layer, and 9-micrometer ultra-thin copper foil, and an insulating adhesive line 2 as example 2 conductor metallic foil 1 Thickness prepared the epoxy system double-sided copper-clad laminate sheet

circuit processed at 0.2mm as AS-6000E (the HITACHI CHEMICAL CO. LTD. make, brand name) and a inner layer board 4 as an epoxy adhesive film whose resin layer is 70 micrometers in thickness. Next, AS-6000E (the HITACHI CHEMICAL CO. LTD. make, brand name) and peeler bull copper foil (the Koga circuit foil incorporated company make, brand name) were laid on top of both sides of the inner layer board 4 at this order, for 60 minutes, pressurization heating was carried out and pressure 2.5MPa and the temperature of 170 degrees C produced the multilevel interconnection board. Next, after tearing off copper foil of the 70-micrometer thickness which is a reinforcing layer, the opening 5 0.1mm in diameter was formed in the surface copper foil coat by the etching method. Next, the non-penetrating hole 11 which irradiates carbon dioxide laser and arrives to the inner layer circuit 3 of a inner layer board was made. Next, the conductive coat was formed in the portion of the insulating adhesive line 2 of the non-penetrating hole 11 as a catalyst for plating with DMS-E processing liquid (made in brass Belc OBERUFUREHIENTEHINIKU Gaea M Bex Haar, brand name). Next, as a plating resist 8, after carrying out the heated roll lamination of FOTEKKU H-W425 (the HITACHI CHEMICAL CO. LTD. make, brand name), the mask pattern which forms a hole with a diameter of 0.3mm including the non-penetrating hole 11 was used and developed [exposed and]. Then, 12-micrometer-thick electroplating was performed to the non-penetrating hole 11 and its circumference, and exfoliation removal of the plating resist 8 was carried out. Furthermore, etching resist was newly formed, the mask pattern was used and developed [exposed and] in the form of the outer layer wiring 10, the circuit of the outermost layer was formed by the etching method, and the multilayer board of four layers was produced.

[0023] Accumulating the insulating adhesive line 2 and the copper foil coat on both sides further by using the substrate of example 3 example 2 as the inner layer board 4, using the same thing, other material repeated the same process as an example 2, and produced the multilayer board of six layers.

[0024] In comparative example 1 example 1, after giving the catalyst 7 for plating, electroplating was carried out, without forming the plating resist 8. Then, the same circuit as an example 1 was formed.

[0025] Comparative evaluation of the substrate produced by the above example and comparative example was carried out. By the circuit pattern prepared in each substrate, although there was no defect of a short circuit and disconnection in an example 1, 2, and 3 about the portion whose wiring rules are a line / space =50micrometer / 50 micrometers, in the comparative example 1, poor disconnection occurred frequently as simplistic. The hot oil examination (cycle examination done by repeating dip and room temperature underwater 10-second dip for 260-degree-C hot oil 10 seconds) which is one of the reliability tests by the specimen which connected 100 IVH(s) in series In addition, the time at 50 cycle ****** and the

time, Any specimen of change of resistance was good within 10%.

[0026]

[Effect of the Invention] As explained above, manufacture of the multilevel interconnection board in which high-density detailed wiring is possible is attained by this invention. Moreover, in order to make a non-penetrating hole by laser, a diameter can process the diameter of minute of a 100-micrometer level. Furthermore, since the insulating adhesives layer can use the general insulating material used for multilayer printed circuit boards, it can use an insulating material properly according to a use.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) - (h) is a sectional view in each process for explaining one example of this invention, and (a') is a sectional view in one process of other examples of this invention.
[Drawing 2] It is the sectional view showing the multilevel interconnection board manufactured by the method of the example of further others of this invention.
[Explanations of letters or numerals]
1. Conductor Metallic Foil 2. Insulation Adhesive Line
3. Inner Layer Circuit 4. Inner Layer Board
5. Opening 6. Laser Light
7. Catalyst for Plating 8. Plating Resist
9. IVH 10. Outer Layer Wiring
11. Non-Penetrating Hole Insulation Adhesive Line with 12. Conductor Metallic Foil
13. Plating 14. Penetration Hole

[Translation done.]

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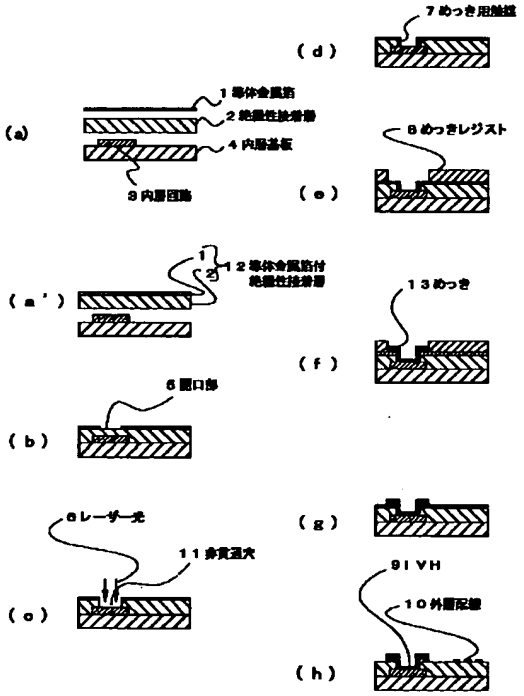
(54)【発明の名称】　多層配線板の製造法

(57)【要約】

【課題】特殊な絶縁材料を用いず、多大な設備投資を必要とせずに配線の高密度化が可能な多層配線板の製造法を提供する。

【解決手段】内層回路３を形成した内層基板４の表面に、絶縁性接着層２と導体金属箔１とをこの順に重ね、加圧加熱して一体化し、導体金属箔１と内層回路３の電気的接続を行うＩＶＨ９を形成する箇所に開口部５を形成し、その開口部５にレーザー光６を照射して非貫通穴１１をあけ、めっき用触媒７を付与し、導体金属箔１の表面に、非貫通穴１１とその周囲を除いて、めっきレジスト８を形成し、めっきレジスト８が形成されていない箇所にめっき１３を行い、めっきレジスト８を除去し、導体金属箔１の不要な箇所をエッチング除去して、外層配線１０を形成する工程を含むＩＶＨ９を持つ多層配線板の製造法。



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【特許請求の範囲】

【請求項1】隣接する層間のみを接続するためのＩＶＨ（９）を持つ多層配線板の製造方法において、以下の工程を含むことを特徴とする多層配線板の製造法。

ａ．内層回路（３）を形成した内層基板（４）の表面に、絶縁性接着層（２）と導体金属箔（１）とをこの順に重ね、加圧加熱して一体化する工程、

ｂ．導体金属箔（１）と内層回路（３）の電気的接続を行うＩＶＨ（９）を形成する箇所の、導体金属箔（１）をエッチング除去して開口部（５）を形成する工程、

ｃ．導体金属箔（１）に形成した開口部（５）にレーザー光（６）を照射して、絶縁性接着層（２）に、内層回路（３）が露出するまで非貫通穴（１１）をあける工程、

ｄ．少なくとも、非貫通穴（１１）内壁の絶縁性接着層（２）に、めっき用触媒（７）を付与する工程、

ｅ．導体金属箔（１）の表面に、非貫通穴（１１）とその周囲を除いて、めっきレジスト（８）を形成する工程、

ｆ．めっきレジスト（８）が形成されていない箇所にめっき（１３）を行う工程、

ｇ．めっきレジスト（８）を除去する工程、

ｈ．導体金属箔（１）の不要な箇所をエッチング除去して、外層配線（１０）を形成する工程。

【請求項2】以下の工程を含むことを特徴とする請求項1に記載の多層配線板の製造法。

ａ．内層回路（３）を形成した内層基板（４）の表面に、絶縁性接着層（２）と導体金属箔（１）とをこの順に重ね、加圧加熱して一体化する工程、

ｂ．導体金属箔（１）と内層回路（３）の電気的接続を行うＩＶＨ（９）を形成する箇所の、導体金属箔（１）をエッチング除去して開口部（５）を形成する工程、

ｃ．導体金属箔（１）に形成した開口部（５）にレーザー光（６）を照射して、絶縁性接着層（２）に、内層回路（３）が露出するまで非貫通穴（１１）をあける工程、

ｄ．少なくとも、非貫通穴（１１）内壁の絶縁性接着層（２）に、めっき用触媒（７）を付与する工程、

ｅ．導体金属箔（１）の表面に、非貫通穴（１１）とその周囲を除いて、めっきレジスト（８）を形成する工程、

ｆ．めっきレジスト（８）が形成されていない箇所にめっき（１３）を行う工程、

ｇ．めっきレジスト（８）を除去する工程、

ｈ１．導体金属箔（１）の不要な箇所をエッチング除去して、第1の外層配線を形成する工程、

ｊ．工程ａ～工程ｈ１を必要回数繰り返し、工程ａ～工程ｈを行う工程。

【請求項3】工程ａにおいて、絶縁性接着層（２）と導体金属箔（１）とを重ねることに代えて、これらが一体化した導体金属箔付き絶縁性接着層（１２）を用いることを特徴とする請求項１または２に記載の多層配線板の製造法。

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【請求項4】以下の工程を追加して貫通穴（１４）も同時に設けることを特徴とする請求項1～3のうちいずれかに記載の多層配線板の製造法。

・工程ｂまたは工程ｃに貫通穴（１４）をあける工程、

・工程ｄにおいて、貫通穴（１４）の内壁にもめっき用触媒を付与する工程、

・工程ｅにおいて形成するめっきレジストが、貫通穴（１４）とその周囲においても除かれているように形成する工程、及び、

・工程ｆにおいて、貫通穴（１４）の内壁にもめっき（１３）を行う工程。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、隣接する層間のみを接続するための　ＩｎｔｅｒｓｔｉｔｉａｌＶｉａ　Ｈｏｌｅ（以下、ＩＶＨという。）を持つ多層配線板の製造方法に関する。

【０００２】

【従来の技術】多層配線板においては、従来から層間を電気的に接続する方法としては、貫通穴をあけた後に金属めっきする手法が主流であった。しかし、この方法では貫通穴による配線禁止領域が全層にあるため高密度化の障害となっており、近年は、隣接する層間のみを接続するためのＩＶＨを使用する方式が実用化されてきている。この製造方法としては、特開平４－１４８５９０号公報に記載されているように、内層回路基板の表面に感光性を有する絶縁層を形成し、層間接続を行う部分の基板表面の絶縁層にフォトリソグラフ法で非貫通穴をあけ、その穴及び基板表面を金属めっきした後、基板表面の導体をエッチング法により回路形成する方法（フォトビア法）がある。

【０００３】また、特公平４－３６３７号公報に記載されている様に、金属箔と絶縁性接着剤を、内層回路基板の表面に重ねて積層接着し、層間接続を行う部分の基板表面の金属層にエッチング法で穴をあけ、更にレーザー等で非貫通穴をあけ、その穴及び基板表面を金属めっきした後、基板表面の導体をエッチング法により回路形成する方法（レーザー穴あけ法）もある。

【０００４】

【発明が解決しようとする課題】特開平４－１４８５９０号公報に記載された方法では、絶縁層にはフォトリソ性、絶縁性、めっき金属との接着性、基板への塗膜形成性等の多くの特性が求められることになるが、現在、全てを満たすものは少なく、また、現在の設備だけで行うこともできず、何らかの設備的な投資が必要となる。例えば、絶縁性とフォトリソ性を両立するために、極性基の少ない材料系を選択するとフォトリソ工程の現像にお

いては、溶剤現像を採用しなければならず、環境保護の観点から塩素系溶剤が使えないため、可燃性溶剤を用いて完全防爆型の装置が必要となる。また、特公平4－3637号公報に記載された方法では、金属箔上に更に金属めっきを付けるために導体回路となる金属層の厚みが厚く、エッチング法で回路を形成する場合には、回路の微細化に限界がある。

【0005】本発明は、特殊な絶縁材料を用いず、多大な設備投資を必要とせずに配線の高密度化が可能な多層配線板の製造方法を提供することを目的とする。

【0006】

【課題を解決するための手段】本発明の多層配線板の製造法は、隣接する層間のみを接続するためのIVH9を持つ多層配線板の製造方法において、以下の工程を含むことを特徴とする。

a．図1（a）に示すように、内層回路3を形成した内層基板4の表面に、絶縁性接着層2と導体金属箔1とをこの順に重ね、加圧加熱して一体化する工程、

b．図1（b）に示すように、導体金属箔1と内層回路3の電気的接続を行うIVH9を形成する箇所の、導体金属箔1をエッチング除去して開口部5を形成する工程、

c．図1（c）に示すように、導体金属箔1に形成した開口部5にレーザー光6を照射して、絶縁性接着層2に、内層回路3が露出するまで非貫通穴11をあける工程、

d．図1（d）に示すように、少なくとも、非貫通穴11内壁の絶縁性接着層2に、めっき用触媒7を付与する工程、

e．図1（e）に示すように、導体金属箔1の表面に、非貫通穴11とその周囲を除いて、めっきレジスト8を形成する工程、

f．図1（f）に示すように、めっきレジスト8が形成されていない箇所にめっき13を行う工程、

g．図1（g）に示すように、めっきレジスト8を除去する工程、

h．図1（h）に示すように、導体金属箔1の不要な箇所をエッチング除去して、外層配線10を形成する工程。

【0007】多層化するには、以下のようにすることによって可能である。

a．内層回路3を形成した内層基板4の表面に、絶縁性接着層2と導体金属箔1とをこの順に重ね、加圧加熱して一体化する工程、

b．導体金属箔1と内層回路3の電気的接続を行うIVH9を形成する箇所の、導体金属箔1をエッチング除去して開口部5を形成する工程、

c．導体金属箔1に形成した開口部5にレーザー光6を照射して、絶縁性接着層2に、内層回路3が露出するまで非貫通穴11をあける工程、

d．少なくとも、非貫通穴11内壁の絶縁性接着層2に、めっき用触媒7を付与する工程、

e．導体金属箔1の表面に、非貫通穴11とその周囲を除いて、めっきレジスト8を形成する工程、

f．めっきレジスト8が形成されていない箇所にめっき13を行う工程、

g．めっきレジスト8を除去する工程、

h1．導体金属箔1の不要な箇所をエッチング除去して、第1の外層配線を形成する工程、

j．工程a～工程h1を必要回数繰り返し、工程a～工程hを行う工程。

【0008】また、工程aにおいて、絶縁性接着層2と導体金属箔1とを重ねることに代えて、これらが一体化した導体金属箔付き絶縁性接着層12を用いることもできる。

【0009】さらに、以下の工程を追加して、図2に示すように、貫通穴14も同時に設けることができる。

・工程bまたは工程cに貫通穴14をあける工程、

・工程dにおいて、貫通穴14の内壁にもめっき用触媒を付与する工程、

・工程eにおいて形成するめっきレジスト8が、貫通穴14とその周囲においても除かれているように形成する工程、及び、

・工程fにおいて、貫通穴14の内壁にもめっき13を行う工程。

【0010】

【発明の実施の形態】

（工程a）本発明で使用する導体金属箔1は、エッチング法で配線形成できるものであれば使用可能であり、一般的には銅箔が好ましい。また、微細配線を形成するために金属箔の厚みはできるだけ薄いものが好ましいが、銅箔が単層の場合には、取扱性から考えると9μmから18μmが良い。また、ライン／スペースが50μm／50μm未満の極めて微細な配線を形成する場合には、銅箔の厚さは更に薄いものが望ましく、このような場合には3～9μmの極薄銅箔とその極薄銅箔の強化層からなる複合箔を使用する。この強化層は加圧加熱積層後に、引き剥がしによって剥離するか、もしくはエッチングによって除去する。引き剥がし可能な複合箔の例としては、70μm厚さの銅箔と9μmの極薄銅箔からなるピーラブル銅箔（古河サーキットホイル株式会社製、商品名）がある。エッチングによって強化層が除去できるものとして、アルミニウム箔に5μmの極薄銅箔を複合化したアルミニウム箔をエッチングで除去する複合箔（三井金属工業株式会社製）等がある。

【0011】本発明で用いる、絶縁性接着層2の樹脂としては、フェノール樹脂、エポキシ樹脂、ポリイミド樹脂などの樹脂が使用できる。この絶縁性接着層2は、内層基板4に加圧加熱して積層後、レーザー光6を照射して層間接続のための穴をあけるので、層間接続の直径を

越える無機質繊維がこの絶縁性接着層２に含まれていると、レーザー加工に要する時間が長くなり生産性が著しく低くなるため、この絶縁性接着層２にはレーザー光６であける穴の直径以上の長さの無機繊維を含まないことが望ましい。絶縁性接着層２としては、エポキシやポリイミド類を成分として含むものであり、例えば、分子量１０万以上の高分子量エポキシ重合体を主成分としたエポキシ系接着フィルムとして、ＡＳ－３０００Ｅ（日立化成工業株式会社製、商品名）がある。変成ゴムを添加したエポキシ系接着フィルムとしてＧＦ－３５００（日立化成工業株式会社製、商品名）がある。ポリイミド系接着フィルムとしてはＡＳ－２５００（日立化成工業株式会社製、商品名）がある。直径が０．１～６μｍで長さが約５～１００μｍの繊維状物質をエポキシ系樹脂中に分散させたエポキシ系接着剤フィルムとして、ＡＳ－６０００Ｅ（日立化成工業株式会社製、商品名）がある。これらの絶縁性接着層２は引き剥がし可能なフィルム上に、熱硬化性樹脂を溶剤に溶解したワニスを塗布した後、溶剤分を乾燥することによって得られる。この絶縁性接着層２の厚さは内層回路３の厚さと関係しており、内層回路３の充填性の点から、少なくとも内層回路３の厚さ以上であることが必要である。内層回路３の厚さが１２μｍの場合には、２５μｍ程度の厚さのものにする。内層回路３の厚さが５μｍ程度の薄さであれば、１０μｍ程度でも内層回路３を充填することができる。一般にはこの絶縁性接着層２の厚さは１０～５００μｍの範囲である。

【００１２】導体金属箔１と絶縁性接着層２を重ねることに代えて用いることのできる、導体金属箔１と一体化した導体金属箔付絶縁性接着層１２は、導体金属箔１の表面に上述した引き剥がし可能なフィルムに絶縁性接着剤を塗布したものを貼り合わせ、その後フィルムを引き剥がすことで得られる。引き剥がし可能なフィルムは、有機フィルムが好適であり、接着剤を塗布する有機フィルムとしては、塗布後に溶剤分を加熱乾燥除去するために、この加熱温度での耐熱性が必要である。このような有機フィルムとしては、ポリエチレンテレフタレート、ポリプロピレン、４メチルペンテン１ポリマー、ポリフッ化エチレン等が使用できる。これらのフィルムの厚さは５μｍ以上であり、取り扱い性の点からはある程度の厚さが必要である。このような点から望ましい厚さは１０～７０μｍである。

【００１３】また、この導体金属箔付絶縁性接着層１２は、絶縁性接着剤樹脂を溶剤に溶解したワニスを、直接金属箔に塗布することでも得られる。このような材料としては、例えば、分子量１０万以上の高分子量エポキシ重合体を主成分とした銅箔付エポキシ系接着フィルムとして、ＭＣＦ－３０００（日立化成工業株式会社製、商品名）がある。また、直径が０．１～６μｍで長さが約５～１００μｍの繊維状物質をエポキシ系樹脂中に分散させた銅箔付エポキシ系接着剤フィルムとして、ＭＣＦ－６０００Ｅ（日立化成工業株式会社製、商品名）がある。

【００１４】本発明で使用する内層基板４としては、紙基材やガラス基材を含むエポキシ系、フェノール系、ポリイミド系の片面銅張積層板が使用できる。また、これらの基材と樹脂からなる両面銅張積層板が使用される。これらの基材を使用してエッチング法やめっきとエッチングの両方を用いて内層回路３を形成する。また、紙基材やガラス基材を含むエポキシ系、フェノール系、ポリイミド系基板にアディティブ法で導体パターンを形成したものも使用できる。また、金属基板やセラミック基板等の表面に導体パターンを形成したものも使用できる。内層基板４がその両面に回路を形成した両面回路基板の場合には、層間接続穴は導電性ペーストまたは絶縁性樹脂で充填した両面回路基板を使用する。

【００１５】この内層基板４に絶縁性接着層２と導体金属箔１をこの順に重ね、加圧加熱して一体化する条件は、使用する樹脂に依存するが、一般には１６０～２８０℃の加熱温度範囲で、圧力は一般に１～５０ＭＰａの範囲である。

【００１６】（工程ｂ）導体金属箔１に設ける開口部５の穴径は特に限定するものではなく、基板の高密度化の観点から小さいほど良いが、エッチング法での工程能力やめっき付まわり性等から考慮して、５０μｍ以上が好ましい。

【００１７】（工程ｃ）開口部５に照射するレーザー光としては、エキシマレーザー、炭酸ガスレーザー等があるが、導体金属箔１以外の樹脂層を選択的に加工しやすいこと、加工速度が早くメンテナンスの容易な炭酸ガスレーザーが好適である。レーザー穴あけでは、開口部５の直径より大きなビーム径のレーザー光を照射することで、導体金属箔１の開口部５と同一の場所の絶縁性接着層２に同一の直径の穴をあけて、内層回路３が露出するまで非貫通穴１１をあけることができる。この時のレーザー加工条件は、絶縁性接着剤層の種類により変化するため、予め実験的に最適条件を選択する。

【００１８】（工程ｄ）非貫通穴１１の内壁の絶縁性接着層に、付与するめっき用触媒７は、一般にシーディングと呼ばれている微細金属粒子を析出させる方法や、導電性の皮膜を形成する方法、例えば、ＤＥ３８０６８８４Ｃ１号公報に記載されているように、穴部分の樹脂部分に対し、異原子として窒素又は硫黄を有する５又は６員の複素環基からなるモノマーを吸着させた後、酸化剤により重合させることで、導電性ポリマー層を形成する方法等がある。本発明においては、穴内壁と穴近傍のみをめっきするため、短い工程で短時間に処理可能な電気めっきを併用できる後者の方法が好ましい。また、めっき用触媒７及び金属めっきと穴内部の樹脂層との密着強度を上げて接続部分の信頼性を向上させるために、めっ

き用触媒付与工程の前に穴内部の樹脂層表面を酸化処理するデスミア工程を追加することができる。

【0019】（工程ｅ）導体金属箔1の表面に非貫通穴11とその周囲を除いて形成するめっきレジスト8の穴径は、先に形成した非貫通穴11の穴径と、次に形成するめっきレジスト層に設ける穴との位置合わせ誤差を加算した大きさ以上にする。これ以上小さい穴径の場合、めっき層と導体金属箔1との接合部分が導体金属箔1の穴端面のみとなり、接続信頼性が低下するためである。めっきレジスト8としては、通常のプリント基板に使用されているものが使用でき、例えば、フォテックH－K425、フォテックH－W425（いずれも、日立化成工業株式会社製、商品名）等のドライフィルムが使用できる。

【0020】（工程ｆ）穴あけした部分に金属めっきし、内層回路3と導体金属箔1とを接続するＩＶＨ9を形成する方法としては、特に限定するものではなく、通常のプリント基板で行われる無電解めっき又は電気めっき等が適用可能である。

【0021】

【実施例】

実施例1

導体金属箔付絶縁性接着層12として、銅箔厚さが12μmで、樹脂層厚さが50μm、分子量10万以上の高分子量エポキシ重合体を主成分としたエポキシ系接着フィルムであるMCF－3000E（日立化成工業株式会社製、商品名）、内層基板4として、厚さが0．2mmで回路加工済のエポキシ系片面銅張積層板を準備した。次に、これらを重ね合わせて、圧力2．5MPa、温度170℃、60分間、加圧加熱して多層配線板を作製し、エッチング法で表面の銅箔層に直径0．1mmの開口部5を形成した。次に、炭酸ガスレーザーを照射して内層基板4の内層回路3まで届く非貫通穴11をあけた。次に、めっき用触媒7として、ＤＭＳ－Ｅ処理液（ブラスベルク・オーベルフレヒエンテヒニーク・ゲー・エム・ベー・ハー社製、商品名）によって、非貫通穴11の絶縁性接着層2に導電性の皮膜を形成した。次に、めっきレジスト8として、フォテックH－W425（日立化成工業株式会社製、商品名）をホットロールラミネートした後、非貫通穴11とその周囲を含む直径0．3mmの穴を形成するマスクパターンを用いて露光、現像した。その後、非貫通穴11内部と周囲に12μmの厚さの電気めっきを行い、めっきレジスト8を剥離除去した。更に、新たにエッチングレジストを形成して、外層配線10の形状にマスクパターンを用いて露光、現像し、エッチング法で最外層の回路を形成し2層の基板を作製した。

【0022】実施例2

導体金属箔1として、強化層としての70μm厚さの銅箔と9μmの極薄銅箔からなるピーラブル銅箔（古河サーキットホイル株式会社製、商品名）、絶縁性接着層2として、樹脂層が厚み70μmのエポキシ系接着剤フィルムとしてＡＳ－6000Ｅ（日立化成工業株式会社製、商品名）、内層基板4として、厚さが0．2mmで回路加工済のエポキシ系両面銅張積層板を準備した。次に、内層基板4の両面にＡＳ－6000Ｅ（日立化成工業株式会社製、商品名）及びピーラブル銅箔（古河サーキットホイル株式会社製、商品名）をこの順に重ね合わせて、圧力2．5MPa、温度170℃、60分間、加圧加熱して多層配線板を作製した。次に、強化層である70μm厚さの銅箔を引き剥がした後、エッチング法で表面の銅箔層に直径0．1mmの開口部5を形成した。次に、炭酸ガスレーザーを照射して内層基板の内層回路3まで届く非貫通穴11をあけた。次に、めっき用触媒として、ＤＭＳ－Ｅ処理液（ブラスベルク・オーベルフレヒエンテヒニーク・ゲー・エム・ベー・ハー社製、商品名）によって、非貫通穴11の絶縁性接着層2の部分に導電性の皮膜を形成した。次に、めっきレジスト8として、フォテックH－W425（日立化成工業株式会社製、商品名）をホットロールラミネートした後、非貫通穴11を含む直径0．3mmの穴を形成するマスクパターンを用いて露光、現像した。その後、非貫通穴11と周囲に12μmの厚みの電気めっきを行い、めっきレジスト8を剥離除去した。更に、新たにエッチングレジストを形成して、外層配線10の形状にマスクパターンを用いて露光、現像し、エッチング法で最外層の回路を形成し、4層の多層基板を作製した。

【0023】実施例3

実施例2の基板を内層基板4として、更に両面に絶縁性接着層2と銅箔層を積み上げて、その他の材料は同じものを用い、実施例2と同じ工程を繰り返し、6層の多層基板を作製した。

【0024】比較例1

実施例1において、めっき用触媒7を付与した後、めっきレジスト8を形成せずに電気めっきした。その後、実施例1と同様の回路を形成した。

【0025】以上の実施例及び比較例で作製した基板を比較評価した。各基板に設けた配線パターンで、配線ルールがライン／スペース＝50μm／50μmの部分については、実施例1、2、3共に短絡、断線の不良がなかったが、比較例1においては短絡と断線不良が多発した。なお、直列にＩＶＨを100個接続した試験片で、信頼性試験の一つであるホットオイル試験（260℃ホットオイル10秒ディップと室温水中10秒ディップを繰り返し行うサイクル試験）を50サイクル行ったところ、何れの試験片も抵抗値の変化は、10％以内で良好であった。

【0026】

【発明の効果】以上に説明したように、本発明によって、高密度な微細配線が可能な多層配線板の製造が可能

になる。また、レーザーによって非貫通穴をあけるために直径が100μmレベルの微小径が加工できる。更に、絶縁性接着剤層は多層プリント基板用に使用される一般的な絶縁材料が使用できるため、用途に応じて絶縁材料を使い分けることができる。

【図面の簡単な説明】

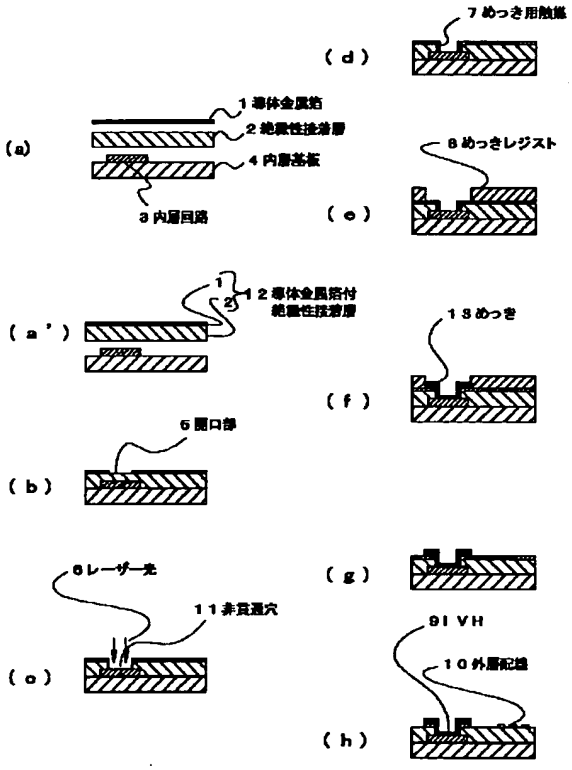
【図1】（a）～（h）は、本発明の一実施例を説明するための各工程における断面図であり、（a'）は、本発明の他の実施例の一工程における断面図である。

【図2】本発明のさらに他の実施例の方法によって製造された多層配線板を示す断面図である。

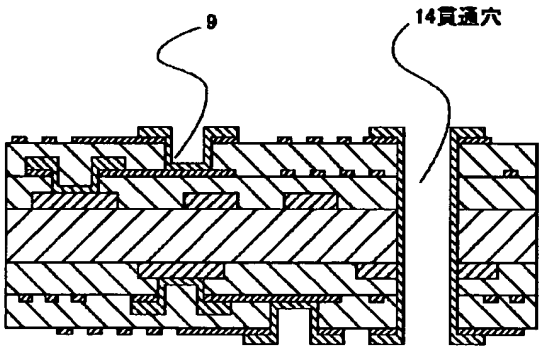
【符号の説明】

1．導体金属箔　2．絶縁性接着層　3．内層回路　4．内層基板　5．開口部　6．レーザ光　7．めっき用触媒　8．めっきレジスト　9．IVH　10．外層配線　11．非貫通穴　12．導体金属箔付絶縁性接着層　13．めっき　14．貫通穴

【図1】



【図2】



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